



FTR THE FINAL TEST REPORT



Vol. 17 No. 11

November 2006

“We’re Undeniably in a Sharp Market Correction” – Mike Bradley, Teradyne

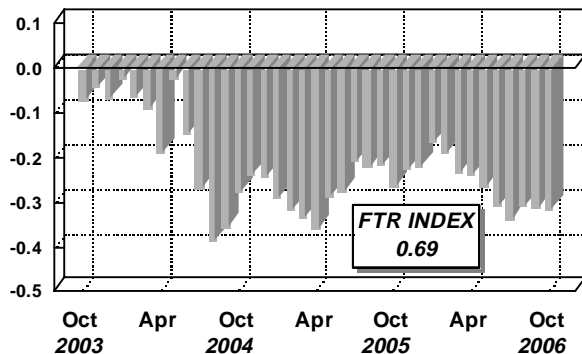
Mike Bradley, Teradyne’s CEO, began his report on his company’s third quarter, ended September 30, by noting that it had quite strong financial results and a series of quarterly records – including free cash flow of \$108 million. Its sales in the quarter of \$359 million were down 8.3 percent from the previous quarter but were up 22.3 percent YoY. Its non-GAAP earnings per share from continuing operations for the quarter were \$0.24/share, and on a GAAP basis, were \$0.33/share. (Its non-GAAP results exclude gains from the sale of real estate and a tax benefit from the sale of TCS, offset to a lesser extent by employee severance charges.) Teradyne ended the third quarter with cash and marketable securities of \$1.147 billion, up \$32 million from the \$1.115 billion at the end of the second quarter. (It retired its remaining convertible debt balance of \$261 million during the present (fourth) quarter.



Mike Bradley

However, Bradley quickly reversed his upbeat presentation by noting that “our bookings in the quarter were down significantly from the second quarter, leading us to guide for lower revenues in Q4.” According to Bradley “the SemiTest industry is clearly in a market correction. After seven straight quarters of increasing orders for our SemiTest products, we saw a drop of 43 percent in orders in Q3 – to \$190 million.” (Semitest sales accounted for 79 percent of its revenue – but its B/B for that sector was just 0.67 in the quarter.

Continued on page 2



FTR’s index of ATE, chipmakers, and PC makers vs. the Dow-30, was unchanged in October even though the Dow set a new high in mid-month.

It also repurchased 8.5 million of its shares at average price of 12.83 totaling \$110 million in the quarter – leaving an authorization of \$290 million remaining. It said its gross margin of 48.8 percent in the quarter was the highest it has ever been on like quarterly sales volume.

INSIDE INFO

	Page
Is ATE Consolidation Req.	3
Global Billings Report	4
Chip Equipment B/B	4
Sept. Qtr. Financial Reports	5
Company Focus-OptimalTest	6
Nextest Magnum iCP CIS	8
LTX Fusion LX	8
New DFT Tools at ITC	9
Advantest F1H Financials	10
ITC Review	11
Freddy’s Test Report	12

Continued from page 1

As a result, he said that in the present (fourth) quarter he expects sales to fall to between \$255 and \$275 million with net/share from continuing operations of just \$0.01 to \$0.05/share.

According to Bradley, the problem was a big pull back by its subcon customers - with orders from that sector in the quarter down about 60 percent sequentially. Orders from its IDM customers were down about half that, about 30 percent he said. Bradley described it as a "sharp correction, similar in many ways to the one in the second half of 2004."

He noted that the 2004 drop was also driven mostly by subcons and both were across a wide range of end markets, applications, and geographies and both occurred as the semiconductor companies were becoming more cautious about their own revenue projections. However, he also noted that SemiTest orders fell about 70 percent - from peak to trough - in the '04 cycle, so this is less than that, although the peak was also less.

However, he noted that there are some important differences between now and two years ago. First, he believes that the subcontract test companies in this cycle have demonstrated much more discipline in managing their assets. They've avoided the heavy over-buying that in the past exacerbated the boom and bust cycles. That increased discipline shows up in their test utilization, which fell off 20 points from their peak in 2004 and so far this year, is down only five or six points.

In addition, there's been virtually no cancellations or pushouts of backlog and short manufacturing cycles and lead times have allowed backlogs to remain secure. In fact, customers are pressing for quick delivery of orders in backlog.

Bradley also cited his favorite "macro indicator" - the industry *buy rate*. That is, the percentage of their revenues that SoC test customers spend on testers.

Bradley calculates that they have spent 2.1 percent of their revenue on test in the first three quarters of this year, slightly up from the 1.9 percent average rate of the last 4 years when annual buy rates ranged from 1.8 percent to 2.1 percent. He believes that they are now trying to bringing that back in line with "a short-term crash diet rather than a prolonged hunger strike." As a result, he believes the industry will likely exit 2006 right on the four-year average of 1.9 percent.

Bradley added, "We're in an environment where customers now get just a bit ahead of the curve, confident that it can quickly correct when needed. As the device industry we serve grows from the mid \$40 billion level per quarter to the \$50 billion level, the quarterly SoC test market goes to an \$800 million to \$1 billion range on an average.

When asked if he expected this be the end of this particular decline, Bradley said that one major change is that equipment acquisition lead times have become shorter that customers can make faster and faster corrections. So, a logical conclusion is that when the adjustment takes place, it likely takes place all at once.

But, he added, "I'm not predicting that we have hit the exact bottom. But I am saying that the market characteristics and the supplier capability allows our customers to move much more rapidly [in either direction] He pointed out that its FLEX and J750 products are basically provided as completed units by its subcontractors. So, it does only final configuration tests at its own facilities, adding boards required to meet a particular customer's requirements. "That now takes less than 60 hours compared to multiple weeks in the past," he said.

When asked if the pull backs happening so quickly worried him about any excess test capacity? Bradley responded "The amount of buying on the up stroke here was less and so there's less worry in the market. Obviously, if chip production goes down then conservatism moves in and that's when things tighten down.

Bradley estimated that the market served by Teradyne's SemiTest product line this year will be about \$3.4 billion. Last year (2005) he put it at about \$2.6 billion. He calculates that if we take both last year's market and this year's and add it together, divide it by two - for those who say last year was slightly low and this year was slightly high - you get \$6 billion, that's a \$3 billion market. Teradyne has about a third of that or \$250 million a quarter. We need about 275 million quarter to hit, in SemiTest, our target model. So we need 10 percent more in share than we have. We've got about a third, we need about 3 points more - around 36 percent.

Although Bradley appeared confident that the above is attainable in the short term, the industry analysts seemed less convinced - and skeptical that even if it was attained, it would not produce the profits for Teradyne that Wall Street is looking for.

The question is, was the fall in Teradyne's chip tester orders at least partially company specific or was it reflective of what happened across the non-memory sector of the global market. It's order fall of 43 percent in the July-September period is over twice what SEMI reported for the TAP industry for that period of about 18 percent. It's possible that large exposure to the subcon market (where it said orders fell by 60 percent QoQ) was a major contributor.

During the analyst question period of the call, Timothy Arcuri of Citigroup, commented "Right now you have lots of cash, cash is about 35 percent of the market cap, when you think strategically about the test business going forward, at about how it grows and might not even grow, in fact at all, are you considering radical moves to get into some of the new technologies that might be eating away at the test business? Because you're sitting there with all this cash and you didn't earn nearly as much as I think many bulls thought you might have."

Bradley responded, "Yes, Tim, we believe that the SoC segment in our position in it gives us the best foundation for earnings growth because of the strategic position, because of the investment rate that's required because of the volatility in the market, which strains all players. So that's the foundation element that is going to give us the earnings growth, the largest piece of the earnings growth. Now, do we think that we can move into other markets? The answer to that is yes. And that would be first of all into segments within SoC that we're not currently playing in and then potentially to leverage technology into other test segments over time. So we're considerably more bullish on the prospects there over the next 3, 4, 5 years. And don't have the view that the buy rate that this market as semiconductors go up that this market is going to stay flat or actually decrease."

That led to Mark Fitzgerald of Banc of America to inquire about the opportunities outside of Teradyne's present core base. He asked, "When you look in the memory market at this point, DRAM and FLASH testers, do you see any of those discontinuities coming up that you could exploit?" Bradley responded; "There are some potential ones in the architecture of next generation memories that we're looking at. The FLEX, high-end FLEX performance has some attributes that may be relevant in the future memory architectures, that's what we're looking at."

Bradley concluded by saying, "I think the correction is a real one. It is a steep correction as has been noted in this conversation. While we observe that it is not as steep as the '04 cycle, that actually to us is not the most defining characteristic. The issue for us is over the cycle profitability and performance. So we're not focusing on what exactly the trough is. We're more focused on the break even structure of the company, the market share momentum, and the gaining of share in the SoC space as the foundation for the future."

IN FTR'S OPINION

Teradyne's third quarter report - described in great detail in the cover article of this issue of FTR, clearly set both financial ana-



lysts' and industry analysts' teeth on edge late last month. Although Teradyne's shares did not suffer a major setback (just 1.9 percent through October 26, other ATE companies - that reported in the week following Teradyne's report - generally did much worse (See table below)

Along with the ATE company downgrades came a new spate of calls from the financial analysts. Mark Fitzgerald of Banc of America Securities, at the analyst panel at ITC last month presented the following chart

Top ATE Providers		
Market Share	2005	2004
Advantest	50%	41%
Teradyne	17%	12%
Verigy	14%	20%
Credence	7%	9%
Others	12%	18%

FTR questions his numbers, but believes that he was trying to make a point - rather than provide information. The point was that the three top players already own 75% of the semiconductor test but only one - Advantest - has the one-third market share. Wall Street (and Teradyne) believes is required for consistent profitability.

ATE Cos. Rpt'g in Late Oct.		
COMPANY	Close 10/27	Change Week
Aetrium	\$3.78	-33.0%
Advantest	\$50.00	-3.2%
Cohu	\$19.82	4.0%
FormFactor	\$37.53	-12.3%
Nextest	\$10.78	-15.5%
Teradyne*	\$13.91	-1.9%

* Two weeks after release

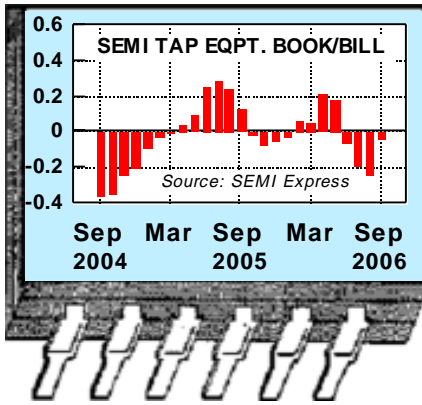
Also late last month a number of other financial analysts, including Mehdi Hosseini, an analyst with Friedman Billings Ramsey, issued bearish outlooks for Teradyne and also urged the ATE industry to consolidate. Hosseini commented, "Most ATE vendors experienced a surge in orders in recent quarters, but are now seeing a slowdown. The ATE industry is falling back into its old and familiar rut, as there are too many IC-test vendors chasing after shrinking capital budgets in a competitive environment. We believe that the industry is in an urgent need of consolidation."

But, do we really need massive consolidation? Would the ATE industry - and its customers - really be better off, if say, Advantest, Teradyne and Verigy were the only viable suppliers of test systems?

FTR does not believe so. The fact is that scenario may have made sense a decade or so ago when chip test was almost entirely a hardware issue. But, those days are gone. Chip test is evolving into a heavily software dependant business as it moves from final testing chips in individual packages to final testing at the die level or in multiple die packages.

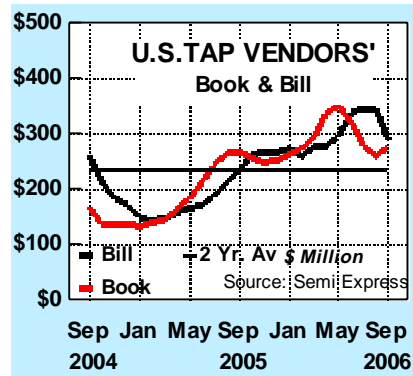
In 2000 this writer was a member of a panel at ITC and there made the case that when consolidation does come to ATE - it will be done by the major EDA companies - not the big iron companies. While I must admit that my premise was not very well received - and I have never been asked back to any ITC panels - my beliefs have not changed. My time frame estimates have slipped a few years, but I still ask how anyone who walked around this year's ITC exhibition and took note of which companies had the big booths - and which companies had none at all - can argue another case?

But, that's still just my opinion!



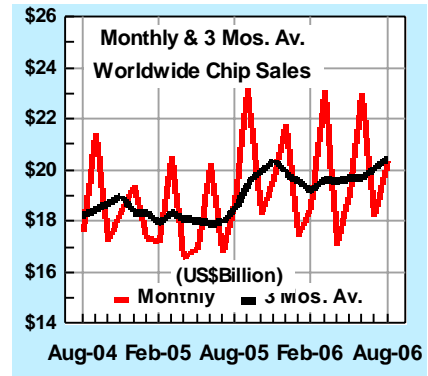
SEMI said that North American chip equipment suppliers reported \$1,624.0 million in bookings (3-month average) for September, down 6.1 percent from the final August bookings of \$1,729.7 million. Total bookings were up 65.0 percent from the level reported one year ago. Total capital equipment billings were \$1,627.4 million in September, 6.6 percent below the final August billings of \$1,742.8 million. The September book-to-bill ratio was 1.00.

Front-end equipment bookings were \$1,346.8 million in September compared with the \$1,471.2 million reported in September and up 87.7 percent from September of last year. September billings were \$1,339.9 million, resulting in a Front-end equipment book-to-bill ratio of 1.01.



TAP equipment bookings were \$277.2 million in September compared with the \$258.5 million reported in August. September billings were \$287.5 million, resulting in a TAP equipment book-to-bill ratio of 0.96. Test Assembly and Packaging equipment August billings were \$343.5 million, while September 2005 billings were \$236.7 million. Bookings in this category were \$266.6 million one year ago, while billings were 236.7 million for a book-to-bill of 1.13.

TAP Book-to-Bill			
US\$ Million			
	Aug'06	Sep'06	Sep'05
Book	\$258.5	\$277.2	266.6
Bill	\$343.5	\$287.5	236.7
B/B	0.75	0.96	1.13



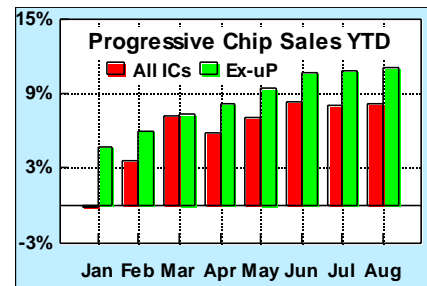
Aug. Actual Chip Sales up 9.0% YoY

The SIA said actual chip sales of \$20.37B set a new record for August, 9.0% above the previous record set in August 2005. Through the first eight months of 2006, total semiconductor sales are now 8.7% ahead of where they were through August 2005. This is a noticeable improvement from what we saw during the first five months of the year, but essentially flat with where we were at the end of June and July, as a result of very unusual sales patterns seen in microprocessors during 2006. If we look at the SIA's numbers, as shown in the graph below, for ICs only (not including discretes, opto-electronics, sensors, and actuators) and with and without microprocessors we find that ICs generally have shown double-digit growth YTD through August.

August 2006 Global Semiconductor Sales

The SIA reported that worldwide sales of semiconductors reached an all-time monthly record of \$20.5 billion (3-month average) in August, an increase of 10.5 percent from the \$18.6 billion reported in August 2005 and up 2.1 percent from July 2006. The previous record for one-month worldwide chip sales was \$20.4 billion in November 2005. "Once again we saw relatively strong sales across a very broad range of semiconductor products, which reflects healthy end markets," said SIA President **George Scalise**. "Sales growth was led by DRAMs, which increased by 7.5 percent from July and by 31.4 percent from August 2005, indicating that PC sales remain strong." *US\$Billion*

Market	Jul'06	MoM		YoY	
		Aug'06	% Chg.	Aug'05	%Chg.
Americas	3.70	3.83	3.6%	3.24	18.3%
Europe	3.17	3.21	1.3%	3.08	4.4%
Japan	3.86	3.92	1.4%	3.60	8.8%
Asia Pacific	9.39	9.58	2.0%	8.67	10.5%
Total	20.12	20.54	2.1%	18.59	10.5%

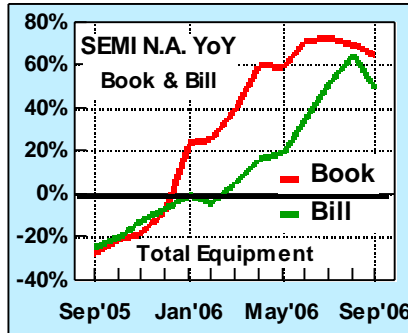


Aug '06 Regional Chip Sales (US\$Billion)			
Market	Aug'06	MoM	YoY
Americas	\$3.94	19.4%	18.2%
Europe	\$3.15	12.8%	6.2%
Japan	\$3.88	4.5%	9.8%
ROA	\$9.40	11.5%	6.2%
TOTAL	\$20.37	11.7%	9.0%

Samsung to Lead Est. '07 CAPEX

Company	2007 (\$M)	YoY%
Samsung	5,758	-17%
Intel	5,400	-7%
Hynix	3,141	-16%
Toshiba	2,825	-3%
AMD	2,500	32%
TSMC	2,000	-25%
IM Flash	1867	-8%
Power Chip	1,831	-15%
Inotera	1,678	102%
SanDisk	1,500	33%
STMicro	1500	-6%
Fujitsu	1,354	-4%
Sony	1,333	-5%
TI	1,300	0%
Micron	1,234	14%
ProMos	1,221	28%
Elpida	1,124	3%
SMIC	1,000	-9%
UMC	1,000	0%
Qimonda	860	13%
IBM	750	0%
Infineon	669	7%
NEC	656	-25%
Renesas	656	-15%
Other	8,343	-3%
Total	51,500	-5%

Source: Pacific Crest Securities.



2006 to be 2nd Best Year for Chip Eqpt.

"The dip in September bookings indicates the current equipment cycle is slowing down," said Dan Tracy, senior director of Industry Research and Statistics at SEMI, last month. September bookings slipped 6.1 percent MoM, but were up 65 percent YoY. Billings fell 6.6 percent MoM, but were up 49 percent YoY. Tracy still believes that the overall performance remains on track to make 2006 the second strongest year for equipment spending in history.

ATE Sales

Advantest and Credence both announced sales of 'open-architecture' testers to NVIDIA on the same day last month. (Both installations had been going on for a while.)

Advantest

Said that NVIDIA has selected T2000 Open-Architecture Test System to support the characterization and debug of packaged silicon products at King Yuan Electronics (Kyec) new production support center in Hsin-chu, Taiwan.

Credence

Said NVIDIA has purchased multiple Sapphire S systems to test products from NVIDIA's handheld GPU and MCP business units" at its key assembly and test subcontractors for use in the manufacture of graphics processor units.

ATE STOCKS

COMPANY	Ticker	Close	Change	52 Week	
		10/31	Month	High	Low
Aehr Test	AEHR	\$5.61	-24.2%	\$11.18	\$3.24
Aetrium	ATRM	\$3.90	-22.6%	\$6.23	\$2.45
Advantest	ATE	\$50.20	0.5%	\$65.20	\$35.76
Cascade	CSCD	\$13.51	8.5%	\$14.81	\$10.80
Cohu	COHU	\$19.78	10.9%	\$29.48	\$14.16
Credence	CMOS	\$3.22	13.0%	\$9.62	\$1.80
Electroglass	EGLS	\$2.91	6.2%	\$5.92	\$2.29
Eagle Test	EGLT	\$17.60	6.5%	\$20.70	\$11.41
ESI	ESIO	\$19.95	-3.2%	\$26.78	\$17.23
FormFactor	FORM	\$38.18	-9.4%	\$49.71	\$23.65
InTest	INTT	\$5.47	-4.7%	\$6.97	\$3.05
K & S	KLIC	\$8.98	1.6%	\$12.50	\$5.99
LTX	LTXX	\$4.67	-6.8%	\$8.00	\$3.26
MCT	MCTI	\$0.22	4.8%	\$0.55	\$0.08
Mosaid \$C	MSD	\$27.85	-3.1%	\$31.50	\$20.15
Nextest	NEXT	\$10.45	-20.6%	\$19.45	\$9.38
Photon	PHTN	\$11.87	-10.6%	\$23.17	\$9.80
Teradyne	TER	\$14.02	6.5%	\$18.08	\$11.50
Verigy	VRGY	\$16.80	3.3%	\$19.52	\$13.55
Avg. Change in Oct. 2006			-2.3%		

FINANCIAL REPORTS

Aetrium Inc.		
Q3 Ending Sept. 30: \$000		
	2006	2005
Sales	\$9,203	\$3,701
Ops Pft.	1,240	(1,024)
Net	1,293	(983)
Per Shr.	0.12	(0.10)

Cascade Microtech, Inc.		
Q3 Ending Sept. 30: \$000		
	2006	2005
Sales	\$22,950	\$18,987
Ops Pft.	1,461	2,169
Net	1,232	2,148
Per Shr.	0.10	0.18

COHU, Inc.		
Q3 Ending Sept. 30: \$000		
	2006	2005
Sales	\$74,787	\$66,823
Ops Pft.	4,692	10,039
Net	4,197	9,562
Per Shr.	0.10	0.48
Orders	76,500	na

FormFactor, Inc.		
Q3 Ending Sept. 30: \$000		
	2006	2005
Sales	\$96,757	\$62,374
Ops Pft.	18,950	8,534
Net	15,819	9,778
Per Shr.	0.33	0.23
Orders	91,000	68,750

Nextest Systems Corp.		
Q3 Ending Sept. 23: \$000		
	2006	2005
Sales	\$26,859	\$17,205
Ops Pft.	6,669	2,418
Net	4,784	1,619
Per Shr.	0.25	0.04
Orders	15,200	na

Teradyne Inc.		
Q3 Ending Sept. 30 : \$000		
	2006	2005
Sales	\$359,122	\$293,573
Ops Pft.	65,346	(40,978)
Net	60,565	(35,378)
Per Shr.	0.31	(0.18)
Orders	239,000	299,000

FOCUS ON OPTIMAL TEST



OptimalTest made its public debut at ITC last month with a large splash. The new company, which designs and builds integrated test management software, introduced its new *Test Management Solutions* – which it describes as “A comprehensive, scalable, and universal software tool for the management of the entire integrated-circuit testing process, from pre-production to post-production.”

The privately held – but apparently well-funded company – was not only the *Diamond Corporate Supporter*, but had perhaps the most impressive exhibition booth at the conference. At that booth, OptimalTest provided live presentations, not only on its new product’s features and benefits but also on industry test management challenges. It offered a series of guest speakers addressing industry test management challenges, including: Bill Price, NXP; Bob Madge, LSI; John Bearden, Consultant; Mike Rodgers, formerly with Intel; Reed Linde, formerly of Intel; Ken Butler, Texas Instruments and Phil Nigh, IBM.



Dan Glotter

Israel-based OptimalTest was founded by Dan Glotter and Nir Erez in early 2005. Glotter, the company’s CEO, before founding the company, had held various managerial positions at Intel from 1994 to 2004 and previously had been a finance manager for a large construction company in Israel. He told *FTR* that he had long been a proponent of adaptive and optimal testing at Intel and has now been able to implement those concepts as the creative vision behind OptimalTest.

The company’s cofounder and COO, Nir Erez, is also one of the owners and founders of Eyrion Group.



Nir Erez

That company is a privately held group of software companies specializing in software localization, mobile communications and CRM implementation. From 2000 to 2003, Nir was founder and CEO of ActionBase, a U.S.-based Eyrion spin-off that provides business management enterprise solutions to enhance internal organizational workflow and collaboration.

A third key employee is Michael Schuldenfrei, VP, Software Development. Before joining OptimalTest in 2005, he was a Senior Software Architect at SAP, where he led the development of Duet, a joint venture with Microsoft to enable seamless access to SAP data via Microsoft Office. Before joining SAP, Michael was a Software Architect at Microsoft and VP, R&D, at ActionBase, a company providing business management enterprise solutions to enhance internal organizational workflow and collaboration.

Optimal’s product is based on the principles of “adaptive testing” that have been known for many years, most broadly in the areas of assessment and training for job skills and academics. The advent of computerization allowed traditional testing to be fine-tuned, so that tests could automatically adjust the level of questioning – easy to difficult – to challenge a person above or below their ability during the actual test process. In effect, computerized adaptive testing (CAT) tailors the test to the ability of the test taker.

In the 1980s, the first academic papers on adaptive testing appeared. Through subsequent decades, patents and commercial applications about adaptive testing applied to semiconductor testing increasingly appeared, and major companies such as IBM and LSI Logic, as well as universities, became thought leaders in the field. Papers on the topic have covered it in the realms of software engineering (open operating system standards); VLSI test (current signatures and adaptive test); and semiconductors (parametric electrical wafer probe).

Notably, in the field of semiconductor testing, adaptive testing figured prominently at the 2004 ITC. There, featured speaker Robert Madge, director of advanced product engineering at LSI Logic, addressed traditional design rules and the constrictions they place on optimized yield. He particularly focused on systematic defects affecting yield, an area that is today more significant than two other kinds of defects, random and parametric. Traditional design rules don’t indicate related yield variations and don’t provide sufficient amounts of statistically valid data for insightful decisions for designers, Madge said.

Madge recommended statistical and adaptive testing with adaptive outlier screening as a more effective test strategy for getting yield feedback into the design flow and extend it even to board and system assembly.

Madge’s position reinforced the view of ITC 2004’s keynote speaker, Bernd Koenemann, chief scientist at Mentor Graphics, who addressed the fact that uncaptured design faults, as well as manufacturing process issues, affect chip yields.

The founders of OptimalTest understood the impact that adaptive testing could have on test management. They also understand how the business environment of the semiconductor industry has changed. Today’s IDMs, foundries, fabless, and assembly test houses) face an end customer who is now predominately in the fast-changing consumer product arena.

So, now device designs are more complex and short-lived than those of the previously dominant IT industry-based devices. Their knowledge about adaptive testing and insight into the semiconductor business environment led them to create what is the company's flagship product, *Optimal Test's Test Management Solutions* (OT-TMS).

Glatter notes that over the last 25 years it was said of IC testing that "you can test all of the defects part of the time and part of the defects all of the time." OptimalTest claims it has "achieved testing of (virtually) all of the defects all of the time." According to Glatter, "Optimal testing is not defined by more testing but rather by correct testing. For example, device edges are more fragile than the center of the IC; therefore, more testing might be appropriate regardless of test results. Stressing – a type of test – is currently done the same way for all types of devices; with optimal testing, one might want to stress more along the device edge."

In addition, he says "Optimal testing is testing that not only is part of the design feedback loop, but it is part of the design-to-production feedback loop – across the entire test process – and it is customized to each device and each type of device."

This new capability has ramifications beyond enhancing yield. It maximizes benefits in the five critical areas – test time reduction, yield, utilization, quality and reliability – that not only affect the quality of the devices themselves but also the financial health and reputation of the semiconductor business operation.

Optimal testing can be layered on top of existing testing infrastructures to realize significant improvements in return on investment of installed technical assets as well as lower overall cost of test. Optimal testing goes beyond principles of adaptive testing for what could be a major step in the evolution of test management software solutions and the robustness of the entire semiconductor industry, or so the company claims.

OptimalTest's Test Management Solutions (OT-TMS) is a totally integrated, automated software solution. The company claims it is applicable to all kinds of devices – SoC, Logic, Memory, Mixed Signal, RF, CMOS Sensors, Stacking CSPs, Mutli Core – from wafer sort to final test. It also says that OT-TMS delivers significant improvements in ROI for existing, installed test technology assets.

Glatter claims the because OT-TMS is customizable, it can add considerable valuable and differentiation to a semiconductor company's devices and process, no matter whether the company is an IDM, foundry, fabless or assembly/test house. It addresses the critical test challenges of test time reduction (TTR), utilization, yield, quality and reliability. By enabling measurable, significant improvements in each of these five key areas, OT-TMS lowers overall test cost of ownership.

OT-TMS delivers significant improvements in ROI for existing, installed test technology assets, according to Glatter. Because OT-TMS is customizable, it can add considerable valuable and differentiation to a semiconductor company's devices and process, no matter whether the company is an IDM, foundry, fables company, or assembly/test house.

OT-TMS addresses the challenges of test time reduction (TTR), utilization, yield, quality, and reliability, enabling measurable improvements in each of these five key areas. OT-TMS delivers seamless connectivity among the five OT-TMS modules as well as with a company's business enterprise systems.

OptimalTest' product is available as a comprehensive suite of test management solutions or modularly, as building blocks. It claims that the OT-TMS delivers seamless connectivity among the five OT-TMS modules and as well can be interfaced with the customer's own business enterprise systems.



OptimalTest's Integrated Test Mgmt. Solutions

The OT-TMS modules are:

- OT-Mgr. The heart of OT-TMS, OT-Mgr provides integrated and coherent management of the multidisciplinary facets of test operations, enabling advanced generation of testing algorithms. OT-Mgr incorporates OT-Rules, the industry's first testing scenario language with easily customizable predefined rule templates.
- OT-Sim. A new industry capability that enables the simulation of testing rules on actual test results prior to implementation in production, OT-Sim helps quantify benefits, schedule monitors and execute what-if scenarios for maximum efficiency and ROI.
- OT-Box. OT-Box is the industry's first real-time, universal station controller for all testers, probers, handlers and test programs. OT-box is totally process- and device-independent, supporting all levels of test parallelism. As part of OT-TMS, it executes rules that have been created and simulated, and implements them for wafer sort and final test in real-time or off-line.
- OT-Post. OT-Post reevaluates all test results to better control the quality and health of all facets of your testing operations. OT-Post performs cross-quality evaluations of the entire testing fleet and all device test-time and yield, offering extreme data integrity. It also augments device reliability through PAT and other advanced outlier detection techniques.



Nextest Systems announced the newest member of its Magnum product line of testers at ITC last month. The *Magnum iCP* is focused on the CMOS Image Sensor (CIS) device market. At ITC it was shown integrated with an AITOS ATS1240 Illuminator and a Semics Opus II wafer probing system.

Nextest says that due to the leveraged power, integration, and cost benefits associated with CMOS technology, CMOS image sensors are finding their way into a myriad of applications ranging from web cams and PDAs, to digital imaging phones and still cameras. Automotive, medical and robotics are all exploring new ways to incorporate these devices into their next-generation products.

As a result, image sensor makers must find alternative test approaches to increase capacity, while decreasing test times and the cost to test these devices. The company claims it now offers the most effective solution to these needs on the market.



Magnum iCP with Semics Prober

The Magnum iCP integrates logic test capability with optimized image capture and analysis hardware. A high-quality light source (illuminator), and a contemporary wafer probing system, provides users with a complete solution for probing up to forty, 256-mega pixel CIS devices in parallel. Nextest claims that this is the highest number of CIS devices being tested in parallel today.

The Magnum iCP can capture pixel data at 100MHz with up to 14 bits per pixel. The Image Capture Ram (ICR) can hold up to 64 image planes. Each of the 40 devices under test has its own image processor, thus providing users with an efficient, high-throughput test solution. Magnum iCP systems are available today with prices starting at approximately \$200,000, depending on configuration.

Tim Moriarty, Nextest's VP of Sales and Marketing commented, "The Magnum iCP system was developed in collaboration with key customers. It responds to their need for a cost effective, high-volume test solution for this rapidly growing marketplace. By utilizing the proven performance of our Magnum product line, we were able to develop a production-worthy test solution in a relatively short time and at a very attractive price."

LTX Unveils New Version of DX Tester

LTX announced its new X-Series Fusion LX test system last month. The LX system builds on the company's desktop DX system - offering more instrument slots, a direct loadboard interface and comprehensive production capabilities - while still maintaining a compact configuration that does not require a mainframe.

The company said that, "This makes the LX ideal for both high volume production and engineering characterization." It offers 20 instrument slots, 128 digital pins, and the X-Series' full range of DSP, DC and power capabilities.



LTX X-Series Fusion LX

This increases the addressable market of the X-series by enabling it to provide a production solution for cost-sensitive analog and low-end mixed signal applications. LTX claims.

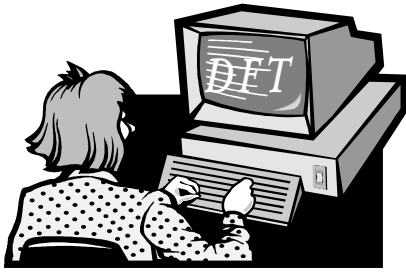
The company's desktop DX test system receive a 2005 *Test & Measurement World Best in Test Award* for semiconductor test," noted Dave Tacelli, CEO/president of LTX.

In conjunction with the unveiling of the Fusion LX, LTX also announced its new PC-based Linux controller for its X-Series test systems. The move to Linux enables customers to run its *enVision* operating system on PCs, both for system control as well as off-line simulation, and also improves test times. LTX offers easy migration to Linux for customers currently running on Solaris/UNIX, and will continue to provide support for Solaris/UNIX, it said.

"In surveying our customers, it was clear that a move to a PC-based system controller was an important requirement," noted Bruce MacDonald, VP of product marketing "After an extensive evaluation, we selected Linux - a powerful, stable platform for our *enVision* operating system.

Linux PC-based system controllers are available now for all new X-Series test systems, and are fully integrated with a new high-speed bus to offer enhanced system performance, including a reduction in typical test times. Specially configured off-line simulation systems are also available.

For existing X-Series systems, an upgrade package is available to allow LTX's customers to migrate current systems.



New DFT Software Tools at ITC

All of the major EDA companies rolled out their latest DFT and DFM tools at ITC last week. The following were some of them.

Synopsys

Synopsys announced that it has collaborated with the *Semiconductor Technology Academic Research Center* (STARC), a research and development consortium founded by major Japanese semiconductor companies with several semiconductor firms to test a new automatic test pattern generation (ATPG) technology designed to increase the quality of manufacturing tests by targeting small delay defects. The enhanced capability uses precise timing information from the Synopsys *PrimeTime* sign-off static timing analysis tool to test for small circuit delays that could result in timing failures when parts are run at speed. It claimed that because traditional transition-delay ATPG does not directly target small delay defects, the new approach can further improve quality and reduce test escapes for digital integrated circuits (ICs) sensitive to small delay defects. Reports and histograms provide metrics for measuring the test quality of a design in the presence of small delay defects. The new ATPG technology is consistent with existing design for test (DFT) methodologies and does not require changes to a design, it said.

Synopsys and Virage Logic

These two companies rolled out a comprehensive test reference flow that links Synopsys' *Galaxy Platform* with Virage Logics *STAR Memory System* for cost-effective testing and repair of embedded memories for system-on-chip (SoC) designs.

The validated test design flow for 90-nm and 65-nm processes "provides designers an automated, comprehensive solution to address time-to-market pressures and challenges of creating high-quality manufacturing tests for complex designs that contain multiple embedded memories," according to the companies.

They also said that the collaboration will continue with a second validated Galaxy test reference flow, which will integrate the testing of Synopsys *DesignWare* IP memories within Virage Logic's STAR Memory System.

Mentor Graphics

Mentor announced the release of the *TestKompress 2007* - an enhanced version of the tool that introduced scan test pattern compression to the marketplace. It said the TestKompress 2007 product offers significant improvements in the most important aspects of automatic test program generation (ATPG) - productivity, performance and test quality.

TestKompress 2007 now comes with a new user interface called *DFTVisualizer*, a graphical environment for managing the complexity of debugging DFT related issues. DFTVisualizer includes several new graphical utilities, including hierarchical design and schematic viewers as well as waveform views that allow users to traverse the design data to pinpoint test related problems. These utilities are tightly coupled with its ATPG Accelerator and the design rule checks. ATPG Accelerator is available to all current TestKompress or *FastScan* customers.

Mentor Graphics also said that its *YieldAssist* tool now supports an automated server-based use model for high volume diagnosis of wafer test failures. With the ability to quickly and accurately identify and isolate yield-limiting defects, it takes failure information directly from manufacturing scan test, and through advanced diagnostics, identifies failure causes.

With this new functionality, YieldAssist is now a fully automated diagnosis job server that monitors multiple directories for failure logs from Automatic Test Equipment (ATE) and manages the diagnosis runs and resources. The server dispatches jobs to machines running diagnosis, balancing the load for maximum throughput. Results are collected into a database for future analysis and reporting. The system is fault tolerant, restarting or removing diagnosis machines that have become unavailable, and marking the queue for easy stop and restart. Furthermore, volume diagnostics is architected in a way that ensures no loss in accuracy, whether processing one failing die or 10,000, Mentor said.

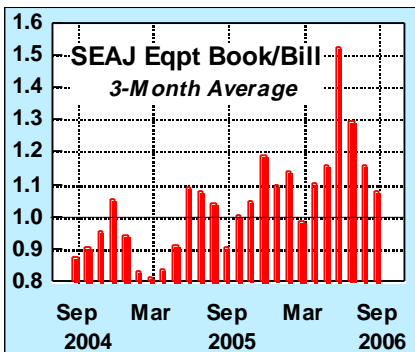
Cadence Design Systems

Cadence introduced the *Cadence Logic Design Team Solution*, which allows concurrent RTL design, enabling schedule predictability. It integrates technology from its *Incisive* functional verification and *Encounter* digital IC design platforms. It integrates design, early verification and front-end implementation tasks into a set of objective-focused sub-flows, and automates the concurrent management of the design's progress toward these objectives.

It takes a concurrent 'Design with' approach as opposed to serial and iterative design. The architecture includes four major elements and an overall plan-to-closure management and logical sign-off solution, while leveraging industry-standard formats such as *SystemVeri-log*. It also integrates test with the logic-design environment to develop and debug high-quality test infrastructure with minimal iterations, Cadence said.

EDA STOCKS

COMPANY	Ticker	Close	Change	52 Week	
		10/31	Month	High	Low
Cadence	CDNS	\$17.86	5.3%	\$19.65	\$14.93
LogicVision	LGVN	\$0.98	-25.8%	\$2.00	\$0.87
Mentor	MENT	\$16.87	19.8%	\$16.46	\$8.02
Synopsys	SNPS	\$22.51	14.1%	\$24.25	\$17.07
Avg. Change in Oct. 2006			3.4%		



Japan Sept. Eqpt. Book-to Bill at 1.08

The SEAJ reported that Japan-based manufacturers of semiconductor equipment posted ¥168,814 million (US\$1,453.6 million) in orders in September (3-month average basis) and a B/B of 1.08. The bookings figure was up 0.9 percent from the final August 2006 level of ¥167,390 million and up 41.1 percent from the ¥119,681 million in orders posted in September 2005. The 3-month average billings in September 2006 was ¥156,292 million (US\$1,345.7 million), up 8.3 percent from the final August 2006 level of ¥144,313 million and 18.0 percent up from the September 2005 billings level of ¥132,465 million.

JAPANESE ATE STOCKS

INDEX	TICKER	Close	Change
		09/29	Month
NIKKEI 225	N225	16,399	4.9%
Advantest	6857	5,910	0.9%
JEM	6855	2,840	-1.4%
MJC	6871	3,320	3.4%
TEL	8035	8,740	0.1%
TSK	7729	5,650	-8.9%
Yokogawa	6841	1,605	3.4%
Average Change in Oct. 2006			-0.4%

Advantest Q2 Sales Flat, Orders Down

Advantest reported that its group net profit surged 51.9 percent (in Yen terms) YoY in the half-year April-September period as its sales grew just 12.5 percent YoY. It reported a net profit of ¥22.20 billion (US\$192.5 million) compared with ¥14.61 billion (US\$132.7 million) a year earlier. Its sales for the half were ¥120.49 billion (US\$1,045 million) up from ¥107.10 billion (US\$973.6 million) during the same period in 2005. Its orders for the half year were down about 5 percent at ¥115.2 (US\$999 million) compared to ¥121.6 billion (US\$1,105 million) in the 2005 period.

However, for the current fiscal year ending March 2007, it lowered its earnings forecast from what it said in its FQ106 report to net of ¥43 billion (US\$372.9 million) on full fiscal year sales of ¥255 billion (US\$2,211 billion) as it became more cautious about the demand and supply conditions in the chip market.

Full Fiscal '06 Forecast (Millions)

(FYr. Ending Mar. 31, 2007)

Sales	US\$2,195.7
Ops. Pft.	US\$560
Net Pft.	US\$ 370.2
Orders	US\$2,109.6

Advantest did not include information on its second fiscal quarter (July - Sept.) in its latest financial report, so the following is based on its first fiscal quarter data - in dollar terms - as reported in *FTR*'s August '06 issue. Advantest's second fiscal quarter sales were about flat QoQ, at US\$522 million, but were up about 10 percent from the same quarter of 2005.

Advantest Corp.

FQ2 Ended Sept. 30 : \$000

	2006	2005
Sales	\$522,000	\$474,400
Ops Pft.	136,600	94,100
Net	92,300	58,400
Orders	433,100	523,500

Its operations profit of US\$136.6 million fell 4.3 percent QoQ, but was up 45 percent YoY. Its net profit of US\$92.3 million was down 7.9 percent YoY, but up 58.1 percent YoY. Its orders declined in the quarter of \$433 million were down 22.5 percent sequentially and 17.3 percent YoY. On October 1, Advantest's Japanese shares were split 2:1, but for the September quarter it earned \$0.49/share on a pre-split basis.

Advantest president, Toshio Maruyama, commented that capital expenditures by U.S. chipmakers such as Intel fell more than expected. However, the company expects to see growth in sales of testers for DRAM in the second fiscal half.

He also said that "in the memory test market demand for front-end test systems was positive in Japan, Taiwan and Korea. However, the results of back-end test systems did not achieve previous forecasts. Sales of test systems for FLASH remained steady. Demand for T2000 SoC testers was low due to a slow down in demand. Sales of LCD driver IC testers was weak in the second quarter as a result of inventory adjustment of LCD panels in Japan and Taiwan."

Maruyama added, "Sales of memory test handler were favorable - particularly for FLASH handlers, while sales of interface products were steady."

1FH Segment Sales (millions)

(US\$ Million)

Memory Testers	S\$407.57
Non Memory Testers	US\$321.72
Hdlrs/Interface	US\$231.53
Service	US\$84.12
Total	US\$1044.94

In the second half of F'06 Advantest said it expects a rapid increase in demand of DDR-2 DRAM used in personal computers, primarily as a result of Microsoft's new Vista operating system early next year. However, it added that it is concerned that restrained capital expenditures as a result of poor supply and demand balance, oil prices, exchange rates and competitive pricing.



The International Test Conference, the center piece of the six-day *Test Week* - finally found its way to San Jose (or more accurately - Santa Clara) CA last month. It's been a long trip, taking 36 years since its beginnings in 1970 in Cherry Hill, NJ. However, it's possible that it may have found a new 'home' at the Santa Clara Convention Center. It will certainly be there for another year and most likely for at least another two years.

It's clear that the Santa Clara facility is an ideal fit for this conference - as close to the center of the chip test industry as there is outside of Asia. There is no question but the attendance - 2365 registered, up 23% YoY and about 600 who visited the exhibits for free- was the best this conference has seen in many years. And, both they and the almost 100 exhibitors seemed very happy with the environment and the great October weather in Northern California.

The conference opened on a high note with all 1,270 seats full for the traditional Plenary session. This year's keynote was given by Nvidia founder and manufacturing manager, Chris Malachowsky, presenting some great graphics tracing the evolution of that technology. (They were particularly enjoyed by the many fans of Saturday morning TV and video gamers - which clearly made up a high percentage of the audience.)



Chris A. Malachowsky

However, he followed it with what he sees as troubling trends in chip testing. He noted that "The costs for a single ASIC [of the complexity of Nvidia's graphics chips] development are growing to over \$46 million with test costs accounting for about \$2 million of the total." He also claims that "as a component of total manufacturing cost, test accounts for about 4-5 percent of the cost."

In addition, he said, "yield costs, which include the costs for final testing and packaging add an additional 5.5 percent to the total costs." He added, "Most of these failures are parts that should have been caught earlier in the production cycle. If the test misses are eliminated, the overall cost reduction would be about 8-10 percent of the current costs. The solution is to increase test quality," he suggested. The cost of testers continues to increase as device complexity and test complexity rise, and the speed and functionality of the chips require larger and faster testers with deeper test memories to handle the full range of test requirements. Overall, test represents about 8 percent of the cost of a final product," Malachowsky said

As usual, ITC resembled a 'five-ring' circus - with multiple papers being presented simultaneously - along with invited talks, lectures and panel presentations. This writer was able to attend only a handful of the papers, some very good, some just fair. (We will try to review some to the 'good' presentations in future issues

No surprise, we attended the *Changing Test Industry: the Analysts' Perspective* panel organized by Amy Gold and moderated by Rochit Rajsuman, of Advantest America,

The panel consisted of two financial analysts - Mark Fitzgerald of Banc of America Securities: and David Egan of Lehman Brothers - and two industry analyst - Risto Puhakka of VLSI Research and Laurie Balch of Gartner:

Both financial analysts advised Semiconductor ATE management to "get consistently profitable or get out!" The industry analysts were more positive. Balch noted that "The test industry is crucial to the success of semiconductor manufacturing and must develop strategies for survival despite constantly changing market dynamics." Puhakka said "ATE suppliers have been confronted by cost-of-test issues for as long as this industry has been in existence. And "Each time the ATE, industry has made significant changes to improve it."

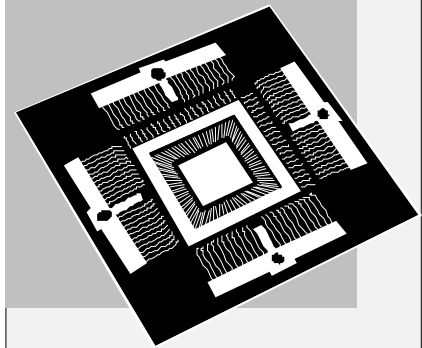
The product exhibition portion was an undeniable success in the view of most of the exhibitors we talked to. The ITC committee again put to rest the old saying that "there's no free lunch" by supplying one each day in the exhibition area along with plenty of tables at which to enjoy it.

The major ATE hardware players, Advantest, Teradyne and Verigy did not exhibit, but the first two bought "Platinum" (\$10,000) sponsorships (as did Mentor Graphics) and got their names in lights all over the conference halls. (Verigy, along with ARM and Test Advantage were Silver (\$5,000) sponsors.

The "social events" including the "Welcome Reception and those of Cadence and in particular Nextest - were very well done and very well attended.

In summary, *FTR* saw ITC'06 as one of its best efforts in years - and we encourage all of our readers to seriously consider joining us in Santa Clara next October for ITC'07.

ATE/DFT MEETINGS



December 6-8, 2006

SEMICON Japan 2006

Makuhari Messe, Chiba Japan

www.semi.org

Jan. 31- Feb. 2, 2007

SEMICON Korea 2007

COEX, Seoul, Korea

www.semi.org

March 11-14, 2007

BiTS Workshop Santa Clara

Hilton East/Mesa, Mesa, AZ

www.bitsworkshop.org



INDUSTRY

Gartner Dataquest lowered its equipment CAPEX outlook for 2006 to 23.5% in 2006, but says the industry will soften in 2007, declining by 2.7%. The industry will rebound in 2008, to growth of 23.3% it said.

- Wafer fab eqpt. revenue will grow 24.6% in 2006, decline, 2.1% in 2007
- The packaging and assembly eqpt. market is forecast to grow 13.6% in 2006, and decline 7.4% in 2007.
- The ATE market will grow 27.4% in 2006, and decline 1.9% in 2007.

Gartner Dataquest, the sole research firm that provided extensive market analysis of the EDA industry, is closing its CAD research group affecting affects five people, including **Gary Smith**, its chief EDA analyst.

iSuppli reaffirmed its forecast for global chip sales, projecting a 7.8% YoY increase \$255.7 billion, virtually any. While maintaining its outlook for 2006, it slightly reduced its outlook for 2007 chip sales to 10% growth, but still said that will be the peak of the present market cycle.

COMPANIES

Kulicke & Soffa Industries, has signed an agreement to acquire **Alphasem**, a supplier of die bonder equipment, from **Dover Technologies**. for about \$30 million.

Aetrium dismissed **PricewaterhouseCoopers LLP** and replaced it with **Grant Thornton LLP** as its independent public accounting firm for the year ending December 31, 2006.

Credence Systems and Canadian-based **Fibics** that specializes in focused ion beam (FIB) applications and analytical services, announced a partnership to provide Credence customers with enhanced, easier-to-use circuit edit (CE) capabilities.

ASM International has decided not to separate its front- and back-end businesses. The company, said it has decided that such a breakup "is not in the best interest of shareholders."

Agilent said its shareholders will receive 0.122435 shares of **Verigy** for each share of Agilent held.

inTEST said its tester interface division, **inTEST Silicon Valley**, launched the Centaur SOC 440 Modular Interface for the Verigy V93000. The new interface is the world's first spring-pin-based tester interface capable of working with 440mm probe cards.

PEOPLE

Dr. Ben Bennetts, founder of **Bennetts Associates**, has retired and transferred his board-level design-for-test (DFT) training and consultancy service to the newly formed **CloverTest Associates** that is made up of the following principals:

- **Joe Kadaras**, formerly of **Asset InterTech** and now founder and owner of **JEK-Tech**, a boundary-scan test accessory and DFT company;
- **Ken Posse**, formerly of **Agilent Technologies** and **Teseda**, who in addition to running his own board-test and DFT consultancy is also chairman of the IEEE P1687 (Internal JTAG) working group.
- **Bernard Sutton**, formerly of **Tera-dyne** and now running his own board-manufacturing and test consultancy.

Gary Sheedy has been named **Advantest Europe's** Engineering Manager, based in Munich.

Edward Bedell was named VP of Quality and Reliability for **ASAT** replacing **Ken Sicz** who resigned for personal reasons. Bedell will be based in Dongguan, China

Edwin J. Gillis was elected to the Board of Directors of **Teradyne**. He most recently served as the senior VP of Administration & Integration at **Symantec**.

Are you reading someone else's copy of this report?

Your customers, vendors, competitors, and co-workers are all reading *The Final Test Report* every month. Isn't time you had your own copy for just \$195.00 per year? We will send you the next two issues with no obligation. You will not be invoiced until after you receive your second issue. In addition, if you include your e:mail address, we will e:mail you the weekly upDATE as well.

Subscribing is easy — just fill-out this form and fax a copy to: 925-906-9427

Or:

Drop your business card into an envelope and mail it to:

IKONIX Corporation
P.O. Box 1938
Lafayette, CA, USA 94549-1938

FTR gives you the information you need — when you need it!

11_06

NAME

COMPANY

TITLE/DEPARTMENT

STREET OR P.O. BOX

MAIL STOP

CITY

ST.

ZIP

E:Mail